CEL California Eastern Laboratories

Evaluation Board Document

NE5550234-EV09-A

Evaluation Board

- Circuit Description
- Typical Performance Data
- Circuit Schematic and Assembly Drawing

Circuit Description

The NE5550234-EV09-A is an evaluation circuit board for Renesas' LDMOS power FET, NE5550234 optimized for the performance at 915MHz. The circuit board is RoHS compliant.

Matching and Bias Circuits

Refer to the schematic and assembly drawing in the two last pages for the component designation and location.

The input matching circuit consists of two sections of low pass network. An inductor, L1 and a section of transmission line, TL4 are the serial components in the network. At output, three sections of transmission line, TL1, TL2 and TL3 provide the required serial components for the impedance transformation. The performance is most sensitive to the length of TL1 and not very sensitive to TL3. The electrical lengths of the transmission lines labeled on the schematic are estimated and for reference only. Some bench tuning on the actual circuit board is usually required to achieve an optimal performance. For applications where there is a constraint on the board space, serial inductors, instead of transmission lines, can be used for the matching circuits. Low loss inductors should be selected to maintain good efficiency of the PA circuit. The resistor, R3(=2.4ohm) at input is used to improve the stability margin. The gain is reduced by about 1-2dB when R3 is used.

LDMOSFETs essentially draw no gate current under normal operation conditions. Therefore a large value resistor, in the order of kΩ, can be used for the bias at gate so that the RF path is completely isolated from the DC line. At the drain an inductor is used as the RF choke. The current rating for this inductor should be high enough to provide the required current at the operation conditions.

Bias Conditions

This evaluation board was optimized at a specific drain voltage, 7.5V. For different supply voltages, the matching circuits should be adjusted to fully utilize the device capability. The quiescent current is 40mA for the data shown below. The gain is higher at higher quiescent currents, particularly when the device is not completely saturated. For many communication systems, where the PA is never at idle state, a high quiescent current might be used.

PCB Material:

The PCB is Getek 28mil two layer board. The dielectric constant of Getek is 4.2.

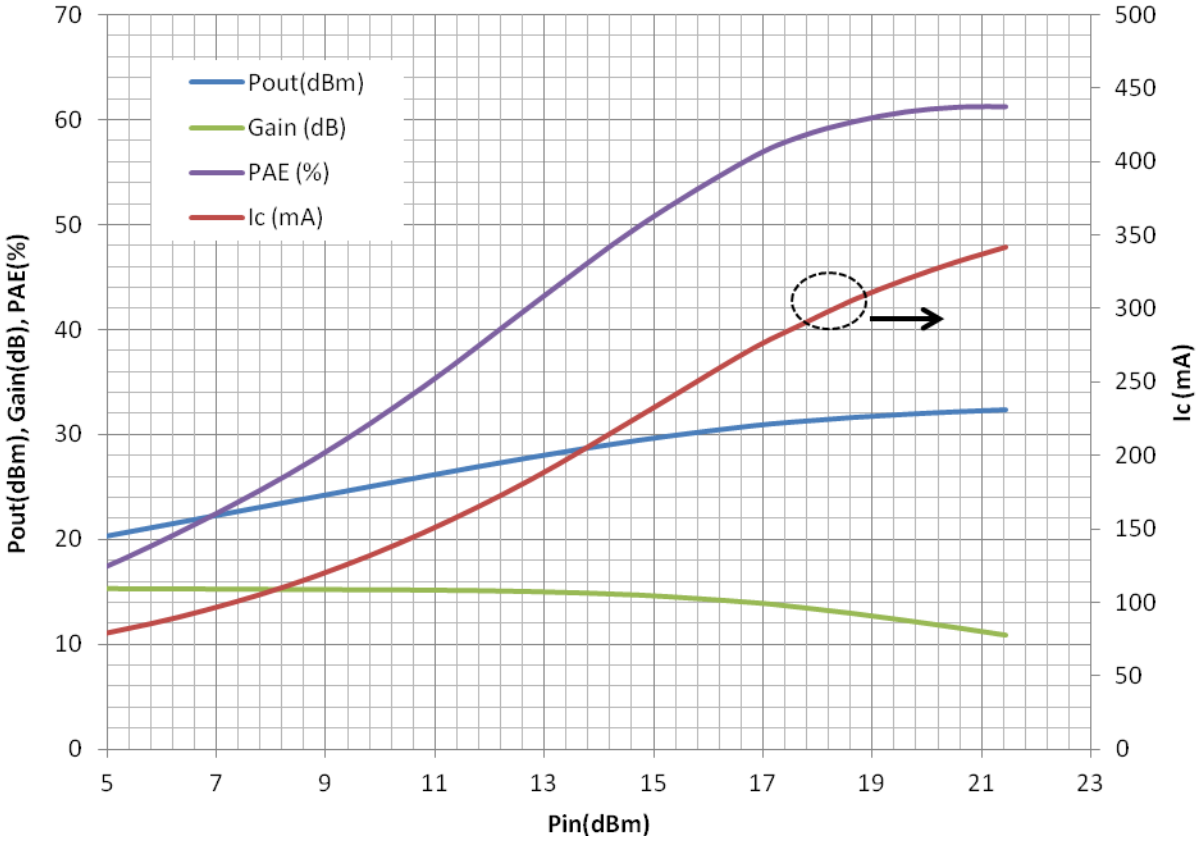
Typical Performance Data

Test Conditions:

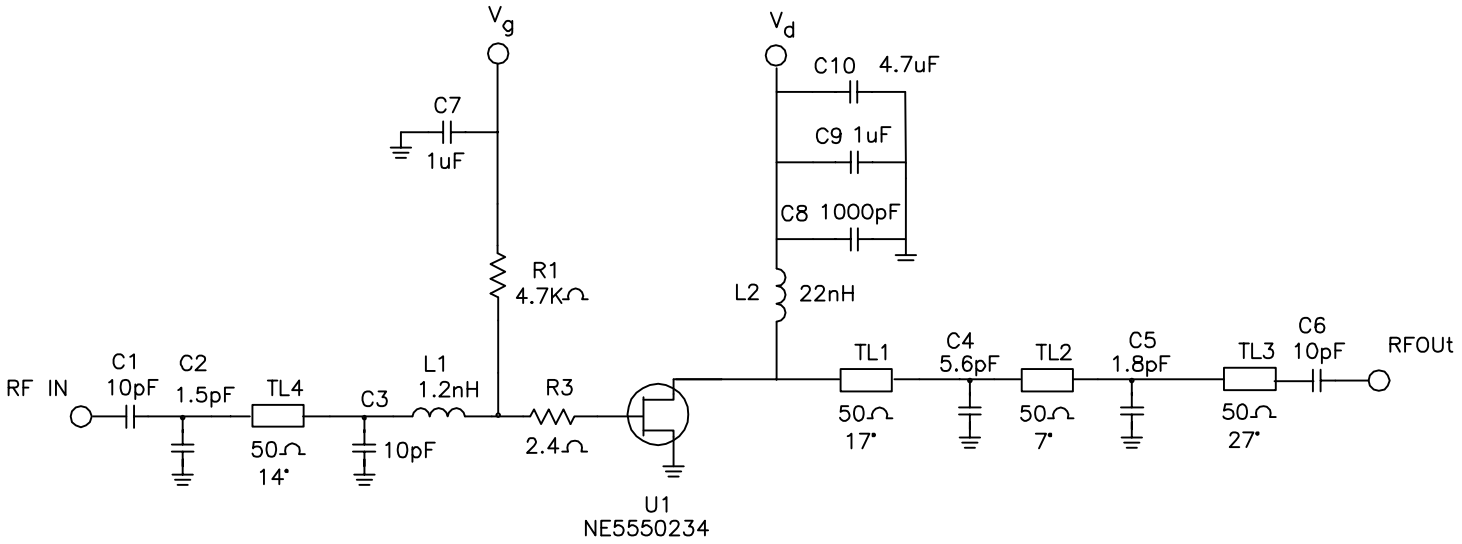
f=915MHz

Vd=7.5V, Idsq=40mA

Pout, Gain, PAE and Current vs Pin are shown in the following plot.



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



Note: All electrical lengths are at 915MHz

ITEM NO.	QTY	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION
17	1	TF-101642		BLOCK
16	1	267M1002475K	C10	4.7uF 10V TANT CHIP CAP b MATS
15	1	GRM1885C1H102JA01	C8	0603 1000pF CAP MURATA
14	2	GRM185R61C105KE44	C7,C9	0603 1uF CAP MURATA
13	1	GRM1885C1H1R8DZ01	C5	0603 1.8pF CAP MURATA
12	1	GRM1885C1H5R6JA01	C4	0603 5.6pF CAP MURATA
11	1	GRM1885C1H1R5DZ01	C2	0603 1.5pF CAP MURATA
10	3	GRM1885C1H100JA01B	C1,C3,C6	0603 10pF CAP MURATA
9	1	GENERIC	R3	0603 2.4 OHM RES
8	1	GENERIC	R2	0603 0 OHM RES
7	1	GENERIC	R1	0603 4.7 KOHM RES
6	1	LQW18AN22NG00	L2	0603 22nH IND WIRE WOUND MURATA
5	2	LQG18HN1N2S00	L1	0603 1.2nH IND MURATA
4	3	1205-003	P1, P2, P3	FEEDTHRU MURATA
3	2	142-0701-841	J1, J2	SMA FEMALE CONNECTOR E.F.JOHNSON
2	1	NE5550234	U1	IC RENESAS
1	1	CL-102046	PCB	COMPONENT LAYOUT DRAWING

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX± .01 .XXX± .005
ANGULAR ± 1°
DO NOT SCALE DRAWING

MATERIAL

FINISH

APPROVALS		
Drawing by:	M Dong	8/16/2012
Designed by:	M Dong	8/16/2012
Checked by:		
Project Engineer:		
Quality Control:		

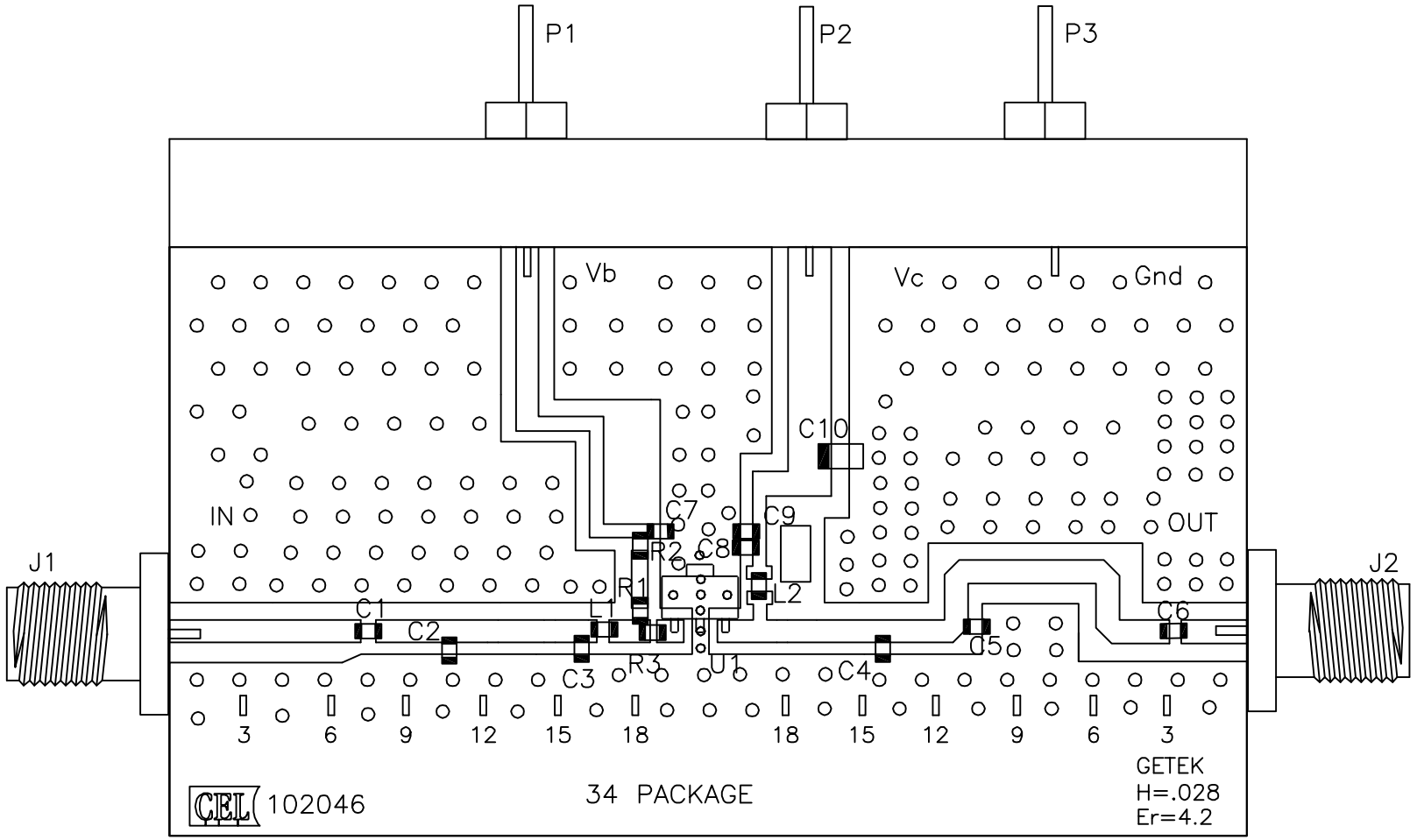
CEL CALIFORNIA EASTERN LABS
4590 PATRICK HENRY DR. SANTA CLARA CA. 95054

TITLE:
NE5550234-EV09-A
SCHEMATIC AND BOM

SIZE	FSCM NO.	DWG NO.	REV
C		AD102066	—

SCALE NONE	RELEASE DATE PROTOTYPE	SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMALS .XX± .01 .XXX± .005 ANGULAR ± 1° DO NOT SCALE DRAWING	APPROVALS	CEL CALIFORNIA EASTERN LABS 4590 PATRICK HENRY DR. SANTA CLARA CA. 95054
		MATERIAL	Drawing by: M Dong 8/16/2012 Designed by: M Dong 8/16/2012 Checked by: Project Engineer: Quality Control:	TITLE: NE5550234-EV09-A LAYOUT
		FINISH		SIZE C · FSCM NO. · DWG NO. AD102066 · REV —
NEXT ASSY	USED ON			SCALE NONE · RELEASE DATE PROTOTYPE · SHEET 1 OF 1
APPLICATION				